WHAT IS CLAIMED IS:

1. A semiconductor device performing drive control of first and second switching devices connected in series and interposed between a high main power potential and a low main power potential, comprising:

a high potential part including a control part configured to control conduction/non-conduction of a high side switching device which is one of said first and second switching devices;

a low side logic circuit provided in a low potential part operating on the basis of said low main power potential and configured to generate a control signal on the basis of a signal applied from outside, said control signal having a first state indicating conduction of said high side switching device and a second state indicating non-conduction of said high side switching device, and to generate first and second pulse signals on the basis of said control signal in correspondence with said first and second states, respectively;

first and second level shift parts configured to level-shift said first and second pulse signals to said high potential part to obtain first and second level-shifted pulse signals, respectively; and

a voltage detecting device provided in said low potential part and configured to detect a potential at an output line of at least one of said first and second level shift parts and to supply a logic value based on the potential for said low side logic circuit, thereby controlling an operation of said low side logic circuit.

2. The semiconductor device according to claim 1, wherein

said voltage detecting device includes:

at least one of a field oxide film and an interlayer insulating film provided in an

upper portion of a semiconductor region which forms a channel region during device operation, as a gate insulating film; and

at least one MOS transistor having said output line provided on said gate insulating film as a gate electrode.

3. The semiconductor device according to claim 2, wherein

said at least one MOS transistor includes an odd number of MOS transistors equal to or greater than three connected in parallel, and

said control signal is controlled on the basis of a logic value which is the majority of outputs of said odd number of MOS transistors.

4. The semiconductor device according to claim 2, wherein

said at least one MOS transistor includes an NMOS transistor and a PMOS transistor constituting a complementary MOS transistor,

said NMOS transistor and said PMOS transistor have said output line as a common gate electrode, and

a logic value of an output of said complementary MOS transistor is supplied to said low side logic circuit.

5. The semiconductor device according to claim 2, wherein

said at least one MOS transistor includes a plurality of MOS transistors connected in parallel, and

said plurality of MOS transistors have different threshold voltages from each other.

6. The semiconductor device according to claim 2, wherein

in said at least one MOS transistors, a semiconductor region including said channel region is electrically insulated from a semiconductor substrate, and

a bias voltage is applied to said semiconductor region to change a potential at said semiconductor region, thereby causing a threshold voltage of said at least one MOS transistor to electrically vary.

7. A semiconductor device performing drive control of first and second switching devices connected in series and interposed between a high main power potential and a low main power potential, comprising:

a high potential part including a control part configured to control conduction/non-conduction of a high side switching device which is one of said first and second switching devices;

a reverse level shift part configured to level-shift a signal from said high potential part to supply the level-shifted signal to a low side logic circuit operating on the basis of said low main power potential; and

a voltage detecting device provided in said high potential part and configured to detect a potential at an output line of said reverse level shift part and to supply a logic value based on said potential for said control part, thereby causing said control part to control conduction/non-conduction of said high side switching device.

8. The semiconductor device according to claim 7, wherein

said voltage detecting device includes:

at least one of a field oxide film and an interlayer insulating film provided in an upper portion of a semiconductor region which forms a channel region during device

operation as a gate insulating film; and

at least one MOS transistor having said output line provided on said gate insulating film as a gate electrode.

9. The semiconductor device according to claim 8, wherein

said at least one MOS transistor includes an odd number of MOS transistors more than two connected in parallel, and

said control signal is controlled on the basis of a logic value which is the majority of outputs of said odd number of MOS transistors.

10. The semiconductor device according to claim 8, wherein

said at least one MOS transistor includes an NMOS transistor and a PMOS transistor constituting a complementary MOS transistor,

said NMOS transistor and said PMOS transistor have said output line as a common gate electrode, and

a logic value of an output of said complementary MOS transistor is supplied to said low side logic circuit.

11. The semiconductor device according to claim 8, wherein

said at least one MOS transistor includes a plurality of MOS transistors connected in parallel, and

said plurality of MOS transistors have different threshold voltages from each other.

12. The semiconductor device according to claim 8, wherein

in said at least one MOS transistor, a semiconductor region including said channel region is electrically insulated from a semiconductor substrate, and

a bias voltage is applied to said semiconductor region to change a potential at said semiconductor region, thereby causing a threshold voltage of said at least one MOS transistor to electrically vary.

13. A semiconductor device performing drive control of first and second switching devices connected in series and interposed between a high main power potential and a low main power potential, comprising:

a high potential part including a control part configured to control conduction/non-conduction of a high side switching device which is one of said first and second switching devices;

a low side logic circuit provided in a low potential part operating on the basis of said low main power potential and configured to generate a control signal on the basis of a signal applied from outside, said control signal having a first state indicating conduction of said high side switching device and a second state indicating non-conduction of said high side switching device, and to generate first and second pulse signals on the basis of said control signal in correspondence with said first and second states, respectively; and

a voltage detecting device provided in said low potential part and configured to detect a potential at an output line extending out of said high potential part outputting said high main power potential and to supply a logic value based on said potential for said low side logic circuit, thereby controlling an operation of said low side logic circuit.

14. The semiconductor device according to claim 13, wherein

said voltage detecting device is provided in a non-provided region of said low

potential part where a semiconductor device operating on the basis of said low main power potential is not provided.

15. The semiconductor device according to claim 13, wherein

said voltage detecting device includes:

at least one of a field oxide film and an interlayer insulating film provided in an upper portion of a semiconductor region which forms a channel region during device operation as a gate insulating film; and

at least one MOS transistor having said output line provided on said gate insulating film as a gate electrode.

16. The semiconductor device according to claim 15, wherein

said at least one MOS transistor includes an odd number of MOS transistors more than two connected in parallel, and

said control signal is controlled on the basis of a logic value which is the majority of outputs of said odd number of MOS transistors.

17. The semiconductor device according to claim 15, wherein

said at least one MOS transistor includes an NMOS transistor and a PMOS transistor constituting a complementary MOS transistor,

said NMOS transistor and said PMOS transistor have said output line as a common gate electrode, and

a logic value of an output of said complementary MOS transistor is supplied to said low side logic circuit.

18. The semiconductor device according to claim 15, wherein

said at least one MOS transistor includes a plurality of MOS transistors connected in parallel, and

said plurality of MOS transistors have different threshold voltages from each other.

19. The semiconductor device according to claim 15, wherein

in said at least one MOS transistor, a semiconductor region including said channel region is electrically insulated from a semiconductor substrate, and

a bias voltage is applied to said semiconductor region to change a potential at said semiconductor region, thereby causing a threshold voltage of said at least one MOS transistor to electrically vary.

20. A semiconductor device performing drive control of first and second switching devices connected in series and interposed between a high main power potential and a low main power potential, comprising:

a high potential part including a control part configured to control conduction/non-conduction of a high side switching device which is one of said first and second switching devices; and

a voltage detecting device provided in said high potential part and inserted between said high main power potential and a node between said first and second switching devices, said voltage detecting device being configured to detect a potential at said node between said first and second switching devices and to supply a logic value based on said potential for said control part, thereby causing said control part to control conduction/non-conduction of said high side switching device, wherein

said voltage detecting device includes at least one MOS transistor whose conduction/non-conduction is controlled on the basis of a potential at an output line extending out of said low potential part outputting said low main power potential.

21. The semiconductor device according to claim 20, wherein

said voltage detecting device is provided in a non-provided region of said high potential part where a semiconductor device operating on the basis of said high side main power potential is not provided.

22. The semiconductor device according to claim 20, wherein

said voltage detecting device includes:

at least one of a field oxide film and an interlayer insulating film provided in an upper portion of a semiconductor region which forms a channel region during device operation as a gate insulating film; and

at least one MOS transistor having said output line provided on said gate insulating film as a gate electrode.

23. The semiconductor device according to claim 22, wherein

said at least one MOS transistor includes an odd number of MOS transistors more than two connected in parallel, and

said control signal is controlled on the basis of a logic value which is the majority of outputs of said odd number of MOS transistors.

24. The semiconductor device according to claim 22, wherein

said at least one MOS transistor includes an NMOS transistor and a PMOS

transistor constituting a complementary MOS transistor,

said NMOS transistor and said PMOS transistor have said output line as a common gate electrode, and

a logic value of an output of said complementary MOS transistor is supplied to said low side logic circuit.

25. The semiconductor device according to claim 22, wherein

said at least one MOS transistor includes a plurality of MOS transistors connected in parallel, and

said plurality of MOS transistors have different threshold voltages from each other.

26. The semiconductor device according to claim 22, wherein

in said at least one MOS transistor, a semiconductor region including said channel region is electrically insulated from a semiconductor substrate, and

a bias voltage is applied to said semiconductor region to change a potential in said semiconductor region, thereby causing a threshold voltage of said at least one MOS transistor to electrically vary.